# 1st mid-term test

**Nanoelectronics – Prof. A. M. Ionescu**
**Examination: Written, Open Books // Duration: 50 minutes**
**Instructions:** Circle only **ONE CORRECT ANSWER** for each question.

# PART I – Nanometer CMOS, FinFETs, and SOI Devices

**Q1. The main motivation for transitioning from planar bulk MOSFETs to FinFETs and FD-SOI transistors in nanometer CMOS nodes is:**

1. To suppress short-channel effects and improve electrostatic control of the channel.
2. To simplify the fabrication process compared to planar devices.
3. To increase the on-current by increasing the gate length.
4. To be able to apply the rules of Dennard scaling.

**Q2. A major difference between FD-SOI and PD-SOI transistors is:**

1. The body of an FD-SOI transistor is thin enough to be fully depleted at threshold.
2. PD-SOI transistors eliminate floating-body effects.
3. FD-SOI devices need much higher operation voltages.
4. PD-SOI devices show lower variability.

**Q3. The back-gate bias in FD-SOI technology is mainly used to:**

1. Improve reliability by lowering the internal electric field.
2. Adjust the threshold voltage dynamically for performance/power trade-off.
3. Reduce the effective oxide thickness.
4. Further deplete the body of the device.

**Q4. For the same channel length and oxide thickness, a FinFET typically shows:**

1. Higher leakage current due to increased electrical fields.
2. The same electrostatic control as planar MOSFETs.
3. Better subthreshold swing and lower DIBL compared to planar MOSFETs.
4. Reduced drive current due to sidewall scattering which lower the mobility.

**Q5. Which factor is a *disadvantage* of FinFETs compared with FD-SOI?**

1. More complex 3D fabrication and lithography.
2. Lack of back-gate bias for threshold tuning.
3. Higher dynamic power due to multi-gate capacitance.
4. All of the above.

**Q6. The effective channel width of a FinFET is approximately:**

1. $W_{eff}=2H_{fin}+T_{fin}$ for a single fin (H= height, T=width of the fin).
2. Equal to the fin height.
3. Determined only by the number of fins connected in parallel.
4. Independent of fin height.

**Q7. In radiation environments, FD-SOI devices are preferred to FinFETs because:**

1. FinFETs are more subject to self-heating.
2. They are cheaper to fabricate.
3. The buried oxide isolates the channel from substrate mobile charge generated by the radiation.
4. The floating body of FD SOI enhances charge collection.

# PART II – Technology Boosters and Tunnel FETs

**Q8. Which of the following *is NOT* typically considered a CMOS technology booster?**

1. Strain engineering.
2. High-k/metal-gate stack.
3. Copper interconnects isolated with low-k dielectrics.
4. Multi-gate architecture.

**Q9. Tensile strain in the channel of a MOSFET primarily enhances:**

1. Threshold voltage control.
2. Electron mobility in n-type devices.
3. Hole mobility in p-type devices.
4. Oxide breakdown field.

**Q10. The main purpose of introducing a high-k dielectric (e.g., $HfO_2$) in both MOSFETs and Tunnel FEts is to:**

1. Decrease oxide capacitance while reducing the gate leakage.
2. Increase gate capacitance while reducing gate leakage
3. Replace silicon dioxide for cost reasons.
4. Compensate for threshold voltage roll-off in scaled MOSFET.

**Q11. The steep subthreshold slope (< 60 mV/dec at 300 K) in Tunnel FETs arises because:**

1. There are no traps at the interface.
2. The device operates in sub-threshold conduction like MOSFETs.
3. The tunneling barrier is temperature-independent.
4. The gate voltage modulates the tunneling probability rather than the carrier energy distribution.

**Q12. Which material properties are desirable for the *source* of a Tunnel FET to achieve high Ion?**

1. Large bandgap and high permittivity constant.
2. Small bandgap and low effective mass.
3. Undoped source, bandgap has minor importance.
4. Highly doped source, bandgap has minor importance.

**Q13. The main challenge limiting the ON-current in Tunnel FETs is:**

1. The limited tunneling probability through the source barrier.
2. The high leakage from the drain.
3. Gate-induced drain leakage.
4. Impact ionization in the channel.

**Q14. Trap-Assisted Tunneling (TAT) in Tunnel FETs:**

1. Improves the subthreshold slope, SS, by adding intermediate energy levels.
2. Has no effect on device performance.
3. Increases the subthreshold swing and degrades steepness
4. Reduces the temperature dependence of the drain current.